METHODS OF FABRICATING A WORD-LINE SPACER FOR WIDE OVER-ETCHING WINDOW ON OUTSIDE DIAMETER (OD) AND STRONG FENCE

FIELD OF THE INVENTION

The present invention relates generally to semiconductor devices and more specifically to split gate flash memory devices.

BACKGROUND OF THE INVENTION

Some flash memory employs an oxide liner to achieve a square profile of its word-line spacer although a fence is formed as a consequence of this method. In order to sustain a higher word-line spacer (for better formation of LDD spacers) and a strong fence (to prevent collapse) it necessary to have less oxide break-through and poly over-etch time which then causes a serious word line bridge issue and particle issues.

In the prior art, the serious bridge issue of the word-line spacers occurs due to insufficient over-etching or producing a weak fence at the side wall of the poly spacer during the break-through etch step.

U.S. Patent No. 6,599,797 B1 to Hofmann et al. discloses and SOI DRAM without a floating body effect.

U.S. Patent No. 5,084,406 to Rhodes et al. discloses a method for forming low resistance DRAM digit-line.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide an improved method of fabricating word-line spacers for split gate flash memory devices.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a substrate having an inchoate split-gate flash memory structure formed thereover is provided. A conductive layer is formed over the substrate and the inchoate split-gate flash memory structure. The conductive layer having: a upper portion and lower vertical portions over the inchoate split-gate flash memory structure; and lower horizontal portions over the substrate. A dual-thickness oxide layer is formed over the conductive layer and has a greater thickness over the upper portion of the conductive layer. The oxide layer is partially etched back to remove at least the oxide layer from over the lower horizontal portions of the conductive layer to expose the underlying portions of the conductive layer. Then etching: away the exposed portions of the conductive layer over the substrate; and through at least a portion of the thinned oxide layer and into the exposed underlying portion of the conductive layer to expose a portion of the inchoate split-gate flash memory structure and to form the word-line spacers adjacent the inchoate split-gate flash memory structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 5 and 8 schematically illustrate a first preferred embodiment of the present invention.

Figs. 1 and 6 to 8 schematically illustrate a second preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Initial Structure Common to Both Embodiments – Fig. 1

Fig. 1 illustrates an inchoate split-gate flash memory structure 12 formed over a substrate 10 common to both embodiments of the present invention that includes a conductive layer 14 formed thereover. Conductive layer 14 is preferably comprised of polysilicon as will be used hereafter for purposes of illustration.

Polysilicon layer 14 has a thickness of preferably from about 1000 to 2000Å, more preferably from about 1250 to 1850Å and more preferably about 1800Å.

Substrate 10 is preferably a silicon substrate or a germanium substrate and is more preferably a silicon substrate.

In the first embodiment, the thickness ratio of upper portion to underlying portion oxide layer may be enlarged with increasing implantation dosage. The ratio could be 1.5 or above. In the second embodiment, the machine limitation leads the ratio only 1.7 or below.

First Embodiment (Implantation of the Upper Portion 15 of Polysilicon Layer 14) – Figs. 2 to 5 and 8

Formation of Dielectric Layer 16 – Fig. 2

As shown in Fig. 2, a dielectric layer 16 is formed over the polysilicon layer 14 of Fig. 1. Dielectric layer 16 is preferably a bottom anti-reflective coating (BARC), a photoresist (PR) layer or a spin-on-glass (SOG) layer and is more preferably a bottom anti-reflective coating (BARC). Dielectric layer 16 has a thickness of preferably from about 2200 to 5000Å, more preferably from about 2500 to 4000Å and most preferably about 3000Å.

Partial Etch-Back of Dielectric Layer 16 – Fig. 3

As shown in Fig. 3, dielectric layer 16 is partially etched back to expose the upper portion 15 of polysilicon layer 14 but leaving the bottom portion of polysilicon layer 14 covered. Dielectric layer 16 is preferably etched back using a plasma etch process or a sulfuric peroxide mixture (SPM) wet bench process or and more preferably using a plasma etch process under the following conditions: about 500 sccm O_2; and about 800 W RF.

Implanting of Exposed Portion 15 of Polysilicon Layer 14 – Fig. 3

As also shown in Fig. 3, an implant 18 is then performed into the exposed portion 15 of polysilicon layer 14 at:

a dosage of preferably from about 1E14 to 5E15 atoms/cm^2 and more preferably from about 1E15 to 5E15 atoms/cm^2;

to a depth of preferably from about 500 to 2000Å and more preferably from about 600 to 1200Å; and

preferably using As atoms or P atoms and more preferably using As atoms.

This leaves portions 17 of partially implanted polysilicon layer 14' unimplanted.

The remaining etched-back dielectric layer 16' is removed to expose the implanted polysilicon layer 14' and the structure is cleaned as necessary. The remaining etched-back dielectric layer 16' is preferably removed using a plasma etch process or a sulfuric peroxide mixture (SPM) wet bench process and more preferably by a plasma etch process.

Growth of Thermal Oxide Layer 20 – Fig. 4

As shown in Fig. 4, an oxide layer 20 is thermally grown over the now exposed partially implanted polysilicon layer 14'. Thermal oxide layer 20 will have a portion 22 of greater thickness over the implanted upper portion 15 of partially

implanted polysilicon layer 14' and will have portions 24 of lesser thickness over the non-implanted lower portions 17. Specifically, thermal oxide layer 20 will have a thickness of preferably from about 200 to 2000Å, more preferably from about 400 to 600Å and most preferably about 500Å over the implanted upper portion 15 and from about 100 to 500Å, more preferably from about 200 to 400 Å and most preferably about 250Å over the implanted lower portions 17.

Partial Etch-Back of Thermal Oxide Layer 20 – Fig. 5

As shown in Fig. 5, thermal oxide layer 20, and the lower horizontal portions of partially non-implanted polysilicon layer 14', are partially etched-back to expose lower vertical portions 28 and lower, partially etched-back horizontal portions 26 of partially etched back, partially non-implanted polysilicon layer 14''. This thins at least the thicker portion 22 of thermal oxide layer 20 to form thinner portion 22' of partially etched-back thermal oxide layer 20' having a thickness of preferably from about 50 to 500Å, more preferably from about 100 to 350Å and most preferably about 120Å. The lower, partially etched-back horizontal portions 26 of partially etched back, partially non-implanted polysilicon layer 14'' each have a thickness of preferably from about 300 to 800Å, more preferably from about 500 to 700Å and most preferably about 600Å.

Etching of Partially Etched-Back, Partially Implanted Polysilicon Layer 14'' – Fig. 8

As shown in Fig. 8, the horizontal portions of partially etched-back thermal oxide layer 20' are completely etched through and then the partially etched-back, partially implanted polysilicon layer 14'' is etched, preferably using an anisotropic plasma etch process, to form the final split-gate flash memory structure 12 having word-line polysilicon spacers 30 with a square profile.

Word-line polysilicon spacers 30 have a width 31 substantially equal to the thickness of formed polysilicon layer 14, i.e. a width of preferably from about 1700 to 1900Å, more preferably from about 1750 to 1850Å and more preferably about 1800Å.

It is noted that remnants 32 of partially etched-back thermal oxide layer 20' remain over the upper, outer side walls of word-line polysilicon spacers 30.

It is also noted that the final structure as shown in Fig. 8, is the same structure for the second embodiment as well as this first embodiment.

Further processing may then proceed.

Second Embodiment (Formation of Poor-Step-Coverage RPO Film 122 Over Polysilicon Layer 14) – Figs. 6 to 8

Formation of Poor-Step-Coverage Oxide Layer 120 – Fig. 6

As shown in Fig. 6, an oxide layer 120 having poor-step-coverage is formed over the polysilicon layer 14 of Fig. 1. Oxide layer 120 is preferably a resist protect oxide (RPO) or low deposition rate (LDR) oxide and more preferably a resist protect oxide (RPO).

Because oxide film 120 is formed having poor step coverage, it will overhang at the top corners of polysilicon layer 14 and will have a portion 122 of greater thickness over the upper portion 115 of polysilicon layer 114 and will have portions 124 of lesser thickness over the lower vertical and horizontal portions 117 of polysilicon layer 114.

Specifically, upper oxide layer portion 122 has a thickness of preferably from about 300 to 700Å, more preferably from about 390 to 610Å and most preferably about 500Å over the upper portion 115 of polysilicon layer 114 and lower oxide layer portions 124 will each have a thickness of preferably from about 180 to 420Å, more preferably from about 250 to 350Å and most preferably about 300Å over the lower portions 117 of polysilicon layer 114.

It is noted that the structure shown in Fig. 6 in this second embodiment is substantially equal to the structure shown in Fig. 4 in the previously described first embodiment. The process key is the deviation between the upper portion 20/22, 120/122 and the underlying portion oxide layer 14.

Partial Etch-Back of Poor-Step-Coverage Oxide Layer 120 – Fig. 7

As shown in Fig. 7, poor-step-coverage oxide layer 120, and the lower horizontal portions of polysilicon layer 114, are partially etched-back to expose lower vertical portions 128 and lower, partially etched-back horizontal portions 126 of partially etched back polysilicon layer 114'''. This thins at least the thicker portion 122 of poor-step-coverage oxide layer 120 to form thinner portion 122' of partially etched-back poor-step-coverage oxide layer 120' having a thickness of preferably from about 50 to 200Å, more preferably from about 100 to 150Å and most preferably about 120Å. The lower, partially etched-back horizontal portions 126 of partially etched back polysilicon layer 14''' each have a thickness of preferably from about 300 to 800Å, more preferably from about 500 to 700Å and most preferably about 600Å.

Etching of Partially Etched-Back Polysilicon Layer 14''' – Fig. 8

As shown in Fig. 8, the horizontal portions of partially etched-back poor-step-coverage oxide layer 120' are completely etched through and then the partially etched-back polysilicon layer 14''' is etched, preferably using an anisotropic

plasma etch process, to form the final split-gate flash memory structure 12 having word-line polysilicon spacers 30 with a square profile.

Word-line polysilicon spacers 30 have a width substantially equal to the thickness of formed polysilicon layer 14, i.e. a width of preferably from about 1700 to 1900Å, more preferably from about 1750 to 1850Å and more preferably about 1800Å.

It is noted that remnants 32 of partially etched-back poor-step-coverage oxide layer 120' remain over the upper, outer side walls of word-line polysilicon spacers 30.

It is also noted that the final structure as shown in Fig. 8, is the same structure for the first embodiment as well as this second embodiment.

Further processing may then proceed.

Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. wide OE window to substrate is led by pre-recessing underlying portion of the polysilicon layer;

2. stronger fence is formed to avoid particle issue with lower oxide breakthrough over etch ratio; and

3. more word-line spacer height is formed to avoid bridge issue, word-line to active area in following cobalt silicide process, by lower over etch ratio on upper portion of the polysilicon layer.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.